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Appl. No. 10/063,779  
Amtd. dated February 17, 2005  
Reply to Office action of November 29, 2004

REMARKS/ARGUMENTS

1. Objection to the specification:

The amendment filed November 2, 2004 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. The amendments to the abstract, and paragraphs

5 0002, 0010, and 0011 are not found in the original disclosure.

**Response:**

The title, the abstract, and paragraphs 0002, 0010, and 0011 have been amended to remove the limitations added in the amendment filed on November 2, 2004. As shown in the Amendments to the Specification section shown above, the title, the abstract, and paragraphs 10 0002, 0010, and 0011 have been restored to their original form. Therefore, reconsideration of the specification is respectfully requested.

2. Rejection of claims 1-5, 7-12, 14-16, and 18-20 under 35 U.S.C. 112, first paragraph:

15 Claims 1-5, 7-12, 14-16, and 18-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims include new limitations "critical dimension of line patterns on a wafer" and "transferring the line patterns of the corrected mask layout to the wafer." These limitations are not found in the original disclosure. Correction is required.

20 **Response:**

The applicant would like to explain how the limitations added to claims 1 and 11 in the amendment of November 2, 2004 are supported in the original disclosure of this application.

25 The first sentence of paragraph 0022 of the original disclosure reads as follows, "Following this, as shown in step 40, a line width correction is made on each of the element pattern types." This establishes that the present invention is

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correcting line widths of element patterns. Additionally, the first sentence of paragraph 0024 of the original disclosure reads as follows, "As shown in Fig.5 and Fig.6, after the element patterns are transferred to a semiconductor wafer, an etched line width of the corrected element patterns A' and B' is in a reasonable range (between 126 nm and 132 nm)." This 5 states that the element patterns with the corrected line widths are then transferred to a wafer.

Claim 1 uses the term "critical dimension" instead of the term "line width", which is used in the two sentences quoted above. However, these terms are used interchangeably in the semiconductor industry. For instance, the applicant has found two online glossaries 10 containing commonly used semiconductor terms. Excerpts from these two glossaries are shown below, along with the Internet URL of the web page from which they came.

Critical dimension, CD: Dimensions of the smallest geometrical features (width of 15 interconnect line, contacts, trenches, etc.) which can be formed during semiconductor device/circuit manufacturing using given technology.

Source: <http://semiconductorglossary.com/default.asp?searchterm=critical+dimension%2C+CD>

Linewidths: The width of a feature printed in resist, measured as a specific height above the 20 substrate. The measurement of the shorter dimension of lines or spaces comprising the patterns formed when manufacturing devices. Also referred to as critical dimension (CD) or feature width.

Source: <http://www.cymer.com/products/glossary.cfm>

25 Therefore, given the support in the specification for correcting line widths of line patterns on a wafer, and given the interchangeable use of "line width" and "critical dimensions" in the semiconductor industry, the amendments made to the preambles of claims 1 and 11 are supported by the original disclosure.

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Additionally, a limitation was also added at the end of claims 1 and 11 stating, "transferring the line patterns of the corrected mask layout to the wafer." This limitation is fully supported by the first sentence of paragraph 0024 of the original specification.

5 In view of the support shown for the amendments made to claims 1 and 11 on November 2, 2004, the applicant respectfully requests reconsideration of claims 1-5, 7-12, 14-16, and 18-20.

3. Interview Summary:

10 A telephone interview was conducted between US Patent Agent Scott Margo (Reg. # 56,277) and the Examiner Saleha Mohamedulla on February 8th, 2005.

15 The topics discussed were the amendments made to claims 1 and 11 and the amendments to the specification. An agreement was made that the added limitation in the amended claims 1 and 11, "transferring the line patterns of the corrected mask layout to the wafer" is supported in paragraph [0024] of the specification as filed.

20 As for the amendments made to the preamble of claims 1 and 11, the applicants will provide definitions from semiconductor glossaries showing proof that the terms "critical dimension" and "line width" can be used interchangably. Upon receiving the reply to the Office action from the applicant, the Examiner will study these definitions along with the specification as filed to determine if the preambles of claims 1 and 11 are sufficiently supported.

25 An agreement was also made to amend the objected paragraphs of specification back to their previous state in order to overcome the objections to the specification.

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Since the objections to the specification have been overcome and since support for the amendments to the claims has been given, the applicant respectfully requests that a timely Notice of Allowance be issued in this case.

5 Sincerely yours,

Winston Hsu

Date: February 17, 2005

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Note: Please leave a message in my voice mail if you need to talk to me. The time in D.C.  
15 is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan).